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Research Article

Design and Analysis of Nanosheet Field-Effect Transistor for High-Speed Switching Applications

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Self-heating effects and short channel effects are unappealing side effects of multigate devices like gate-all-around nanowire-field-effect transistors (FETs) and fin FETs, limiting their performance and posing reliability difficulties. This paper proposes the use of the novel nanosheet FET (NsFET) for complementary metal-oxide semiconductor technology nodes that are changing. Design guidelines and basic measurements for the sub-nm node are displayed alongside a brief introduction to the roadmap to the sub-nm regime and electronic market. The device had an I_{ON}/I_{OFF} ratio of more than 10^5, according to the proposed silicon-based NsFET. For low-power and high-switching applications, the results were verified and achieved quite well. When an NS width increases, although, the threshold voltage (V_{th}) tends to fall, resulting in a loss in subthreshold effectiveness. Furthermore, the proposed device performance, like subthreshold swing I_{ON}/I_{OFF}, was studied with a conventional 2D FET. Hence, the proposed NsFET can be a frontrunner for ultra-low power and high-speed switching applications.

1. Introduction

Mobile devices, computers, and electrical gadgets all store data and instructions in memory, which can be both volatile and nonvolatile. When the power is switched off, the volatile memory erases all information it contains. Nonvolatile memory, on the other hand, keeps all information. Static random-access memory (SRAM) and dynamic random-access memory (DRAM) are two types of volatile memory that store data using transistors and capacitors, respectively. Both SRAM and DRAM can be used interchangeably. Data are stored in nonvolatile memories such as read-only memory (ROM), erasable programmable ROM, and flash memory in an irreversible manner. It can be reconfigured to meet the user's requirements. Engineers seek to reduce power use whenever feasible because it is a scarce resource. Power dissipation reduction is a critical challenge for portable devices. Because memory, particularly cache, is often recognized as the most critical component of any computing device, memory power consumption should be a top focus for any designer. Aggressive technological growth creates large fluctuations in process parameters, resulting in yield, reliability, and testing issues. For every ten degrees of

temperature increase, the failure rate of a VLSI chip is stated to double [1–5].

According to the International Technology Roadmap for Semiconductors (ITRS), memory would consume over 94% of chip space by 2018. According to the ITRS road map, a typical embedded system currently devotes roughly 70% of its transistors to the memory structure, with that percentage expected to climb to 80% in the future [6]. This suggests that when the technology shrinks to sub-32 nm, cache memory leakage will be a substantial source of power loss. The three most crucial metrics to look for if you want a dependable cache memory are read and write static noise margin, as well as hold static noise margin. The static power consumption of an SRAM cell is calculated by adding all transistor leakage currents in the cell [7–10].

In recent years, the most important component of a memory hierarchy computer system has gained significance. SRAM is the most often utilized memory type. Leakage, power, performance, and stability should all be considered when designing SRAM for computer applications [11]. The complementary metal-oxide semiconductor (CMOS) was used to design the cells previously, but CMOS had several difficulties when employed at lower technology nodes, such as leakage currents below the threshold, drain dilation, and gate dilation, all of which were exacerbated by fin field-effect transistor (FinFET). Short-channel effects harm bulk CMOS devices below 45 nm, whereas FinFETs can be used up to the 7 nm technology node without compromising their conducting capacity. Because most circuits are developed in the sub-32 nm size range, MOSFETs are replaced by FinFETs, which eliminate all planner MOSFET's flaws [12]. Over the next few years, developments in processing technology and CMOS scaling will continue to enhance circuit speeds, chip packaging density, and performance-to-cost ratios in microelectronic goods.

Edge effects on the channel's four sides are virtually nonexistent when utilizing a long-channel device. The electric field lines in long-channel devices are always parallel to the channel surface. Gate and back gate voltages control the electric field of semiconductors. Because the channel generates a longitudinal electric field, the drain and source structures are closer to the channel in short-channel devices [13, 14]. When the drain-source voltage is high, the electrical fields travel in a straight line. Between the longitudinal electric field and the direction of current flow, there must be a straight line. If the total depletion widths at both the source and drain are smaller than the channel length, the device is called a short channel device.

As the electric field level declines, the electron drift velocity in the channel increases. When the electric fields are large, these drift velocities become saturated. Velocity saturation is what is going on here. The longitudinal electric field is typically raised in short-channel devices. The MOSFET's I–V characteristics and performance are affected by the phenomenon of velocity saturation, which happens in intense electric fields. When a MOSFET is operated in saturation mode, the saturation current decreases while the gate voltage remains constant. Because of the greater vertical electric field, the channel carriers scatter away from the oxide interface. As a result, the drain current and carrier mobility were reduced.

When the drain voltage is increased, the threshold voltage (V_{th}) is lowered, resulting in short-channel phenomena like DIBL. The carriers will hit a barrier when attempting to reverse the channel's surface unless the gate voltage is larger than the V_{th}. We enhance the gate potential to remove this potential stumbling obstacle. Short-channel devices, on the other hand, are protected by V_{gs} and V_{ds}. The drain voltage must be increased to increase the depletion zone of the drain body.

As a result, even though V_{th} is less than V_{gs}, a reduction of the potential barrier occurs, allowing carriers to travel from the source to drain. DIBL is a drain technique that decreases the V_{th} while lowering the channel barrier. DIBL is a method for solving this problem. V_{th} roll-off is a phenomenon in which the V_{th} lowers as the channel length rises. A subthreshold current will flow when certain conditions occur (off-state current). A spike in drain bias leads the drain current to rise to DIBL even in saturation mode.

When someone punches through it, it has an extreme case of barrier-breaking. The depletion zone around the drain may expand toward the source as the drain bias is increased, resulting in the merging of two independent depletion regions. Region medical term for this illness is punch-through. The drain current will grow too rapidly if the gate voltage is too low, and the gate voltage will lose control. As the channel length shortens, the punch-through strength increases. We cannot turn off the device due to punch-through; therefore, it is no longer useful.

For smaller geometric devices, the electric field becomes significantly stronger towards the drain. The name "electrons" comes from the fact that these heated carriers have a lot of energy (carriers). However, a small percentage of them attain almost enough energy to cause impact ionization at the drain, resulting in more electron–hole pairs being generated. As a result, a drain-to-body current is generated. A gate can trap a few hot electrons tunneling through oxide. Heat carriers, on the other hand, can destroy devices by causing damage to the oxide.

The abovementioned literatures strongly imply how device scaling primarily affects the system level and totally destroys the device. As a result, the device is useless for high-speed and ultra-low power switching applications. For low-power and high-switching applications, the current work focuses on a unique nanosheet tunnel FET (TFET) with different doping concentrations. The device is smaller for an equivalent current with nanosheet FETs (NsFETs), the distance between N and P devices can be lowered because no n-well or polarization is needed, and the intracell interconnects are shorter, which lowers capacitance and resistance. All the researchers explored how to improve device performance by either gate structure modifications by using dual gate or multigate or lightly doped drain implementation or doping effect. But the channel effect was not studied in any of the papers. Therefore, in this study, we have verified all the above challenges and designed NsFET for high-speed switching applications.

2. Background

The introduction of FinFET technology is a major technological trend in the semiconductor industry. Traditional planar transistors have a flat gate and channel, but FinFETs have an elevated channel or "fin." FinFETs have reduced leakage power because of their structure, which allows for higher device densities. FinFETs have a lower V_{th} and higher drive current compared to planar transistors. All of these have the effect of reducing circuit delay, reducing leakage, and increasing performance while taking up less space. FinFETs have a lower cost-per-unit of performance because of this.

With increased device density and driving current in FinFET devices, a higher peak current can be expected. The power grid resistance and package inductance determine the critical voltage drop ($IR + L\,di/dt$) of a large SoC. Planar transistors operate at one volt; therefore, a drop in supply voltage of 100 mV is only a tenth of that voltage. Because of the 100 mV loss, the supply voltage drop is substantially higher for a FinFET with low working voltage. Due to these changes, the chip's operational headroom and noise tolerance are reduced, while high accuracy is required. This incorporates more accurate extraction of the power grid, switching current modeling, and package/PCB impedance accounting [15–18].

The greater current and power density of FinFETs, as well as the smaller connection dimensions, lead to electromigration and higher temperature problems. In terms of device dimensions and cable routing, designers are severely constrained by EM constraints. It leads to thermal issues like self-heating because of the elevated temperature of the FinFETs. Typically, a rise in temperature of 25°C reduces the predicted device and metal layer lifespan by three to five times. It is critical to consider the results of a thorough temperature analysis when trying to pinpoint an object's genuine EM weak point. The mean time to failure decreases as the temperature rises. A close working relationship with a multiple sheet foundry is required for advanced process nodes to meet the foundry's "sign-off" certification requirements using complex EM rules [19].

Using sophisticated FinFET process technology, it is critical to adhere to a power noise mitigation strategy that's been demonstrated in silicon.

2.1. Static IR Analysis. Static EM/IR measurements reflect the overall quality of a power system under normal or DC conditions. Designers can use this check to make sure the power pads and gates are properly planned. It can also assure adequate IP connectivity.

2.2. Power and Signal EM Check. With this, engineers may test their designs to see if the RMS and peak EM restrictions are being met. Current density limitations can be found using EM power and signal tests. Designers can use the results of these tests to size metal segments in accordance with reliability standards.

2.3. Robustness/Connectivity Check. Using an extracted layout, engineers can look for grid weaknesses such as broken vias, short-circuited wiring, and broken via connections on the power straps. This will assist in determining the strength of a cell or block's link to the power and ground grids. With these early inspections, iterations down the design cycle can be completed in less time.

2.4. Vectorless Dynamic Analysis. A multiple-scenario vectorless analysis provides the best sign-off coverage for studying dynamic voltage drop. Using a statistical vectorless engine, engineers can assess a design's sensitivity to many peak current occurrences occurring at the same time. Dynamic voltage drop noise coverage necessitates analyses in all operating modes. Test or scan mode, for example, performs numerous simultaneous switchings even when the frequency is low.

2.5. Low-Power Analysis. If power gates are used, the in-rush current can be checked to make sure it does not exceed the peak current, and coupling noise analysis helps locate hot spots in systems.

2.6. Electrostatic Discharge (ESD) Analysis. The frequency of ESD connection failures increases as the number of process nodes and IPs used in the design decreases. This necessitates resistance and current density analyses based on the layout to find the best clamps and their location. Clamp placement is critical for establishing discharge paths in ESD occurrence.

3. Methodology

The NsFET has more intricate configuration than the MOSFET because of nanosheets stacking. A superlattice of alternating Si and SiGe layers instead of a single channel must be built, and then the selective removal of sacrificial SiGe layers. Between the Si channels, the gate dielectric and metal gate will mount the nanosheets must be placed.

In NS device architecture, providing multi-V_{th} options for designers is substantially more complex than in FinFET or MosFET device architecture. Low V_{th} devices are expended for great performance, while high V_{th} devices are used for low power consumption. To achieve designer goals for an optimal tradeoff between speed and power usage, industrial processes frequently offer up to four different forms of V_{th}. Samsung [20], for example, discussed the launch of sLVT, LVt, RVT, and HVt versions of the same FinFET device in 10 nm technology, with V_{th} changing by 200 mV due to changes in gate stack metal layer thickness between the super-low and high-V_{th} devices. Metal gate boundary control as a method for NsFET multi-V_{th} devices is discussed in [21]. We used different nanosheet thicknesses ranging from 7 to 20 nm in our simulated NsFET. Figure 1 demonstrates a 3D schematic of the recommended nanosheet tunnel FET. Figure 1 depicts a cross-sectional view of NsFET, which was created using Cogenda EDA tool. Many researchers have explored to use FET for various applications [22–31]. Channel length 10 nm with Fin dimension of 10 nm along with two fin's taken for the current study.

4. Results and Discussion

Numerous excellent mechanism structures were developed around the same time that the classical MOS structure was

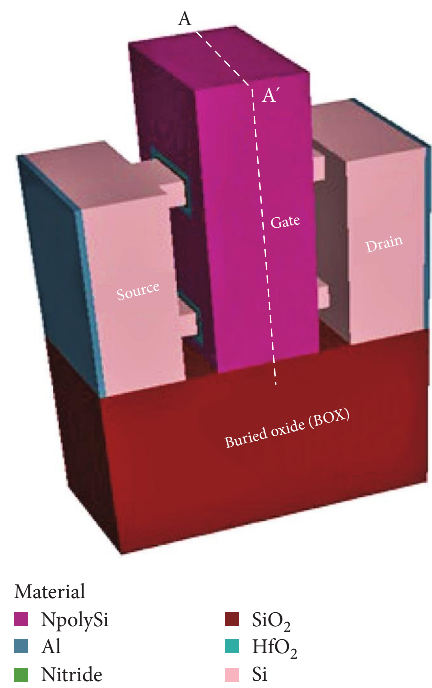

Figure 1: 3D schematic view of proposed nanosheet FET (NsFET).

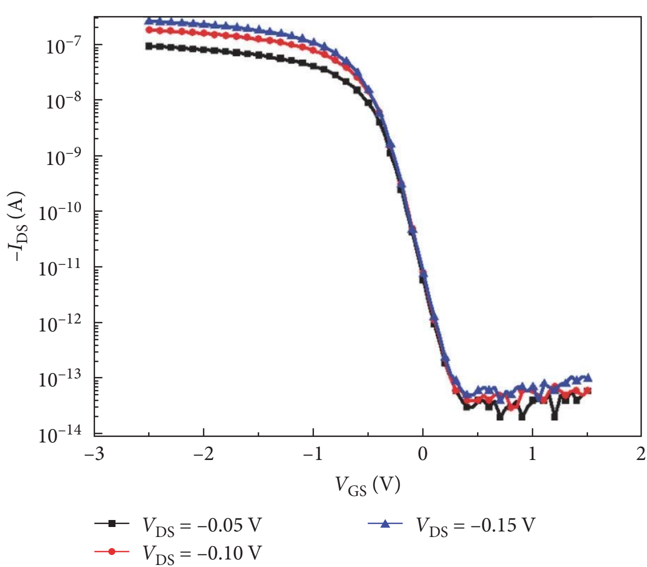

Figure 2: Transfer characteristic of proposed NsFET.

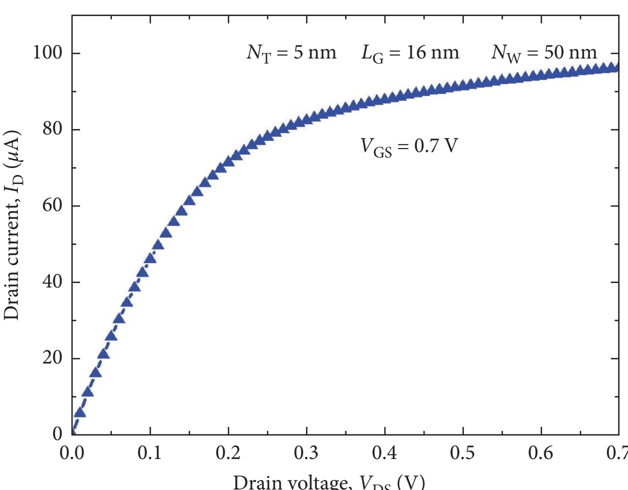

Figure 3: Output characteristics of proposed NsFET.

approaching its scaling limit. Short-channel effects (SCEs) and DIBL are caused by MOSFET scaling, resulting in a decrease in device performance. However. To summarize, the eventual aim of the distinctive semiconductor device is to achieve the highest possible ON current, the highest possible I_{OFF} ratio, and the lowest possible subthreshold slope in order to exhibit a tradeoff between speed and power dissipation. Transconductance, which includes lower source/drain and gate capacitances, a high transconductance to drain current ratio or device efficiency, strong linearity, and low distortion, is how analog circuit quality is calculated. In digital circuits, on the other hand, gate leakage current induced by aggressive scaling of the gate dielectric has a negative impact on the device's efficiency. The model represents the device's electrical characteristics as a function of the device's geometry.

Figure 2 shows the transfer characteristics of the proposed NsFET. The gate voltage (V_{GS}) was varied from 0 to 0.6 V as per ITRS standard. The device structure was created through Cogenda simulator platform. The NsFET is designed with a gate length (L_G) of 16 nm, a fin width of 50 nm, a channel height (H) of 12 nm, and a buried oxide layer of 50 nm. Then the total fin height is $2 \times 12\,\text{nm} = 24\,\text{nm}$. To avoid junction development at nanosized, the device is kept with a consistent doping concentration of $2 \times 10^{18}/\text{cm}^3$. The DIBL and subthreshold swing (SS) are used to assess device efficiency in the subthreshold range. The DIBL and SS are calculated using the formulas [31, 32].

Figure 3 depicts the output characteristics of NsFET. Output characteristics of the device were plotted by keeping the gate to source voltage constant at 0.7 V. Drain characteristic was simulated by varying V_{DS} from 0 to 0.7 V. Potential distribution of the simulated NsFET is shown in Figure 4.

Figure 5 shows the transfer characteristic of simulated 2D FET with varying gate length from 30 to 80 nm at constant V_{DS} of 0.1 V. Transfer characteristic of normal 2D FET was compared with the the proposed NsFET for the same simulation conditions. Transfer characteristic of proposed NsFET has better characteristic for lower channel length, as shown in Figure 6.

Figure 7 depicts the comparison of SS for simulated NsFET with conventional 2D FET for various channel length ranging from 20 to 100 nm. Proposed nanosheet shows better SS for lower channel length as well. The DIBL and SS have been obtained from simulation. The DIBL and SS are obtained using the following formula:

$$\text{DIBL}\left(\frac{\text{mV}}{V}\right) = \left|\frac{(V_{t1} - V_{t2})}{(V_{\text{DS}1} - V_{\text{DS}2})}\right|, \quad (1)$$

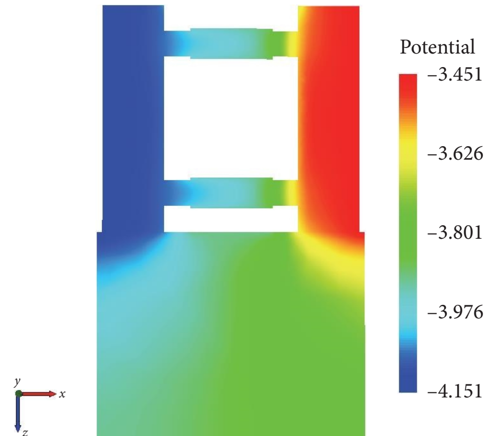

Figure 4: Potential distribution of the simulated NsFET.

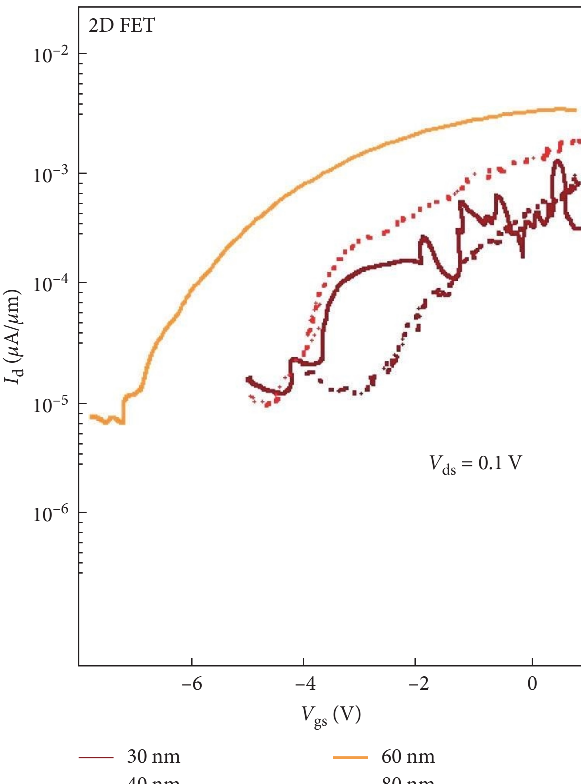

Figure 5: Transfer characteristic of simulated 2D field effect transistor.

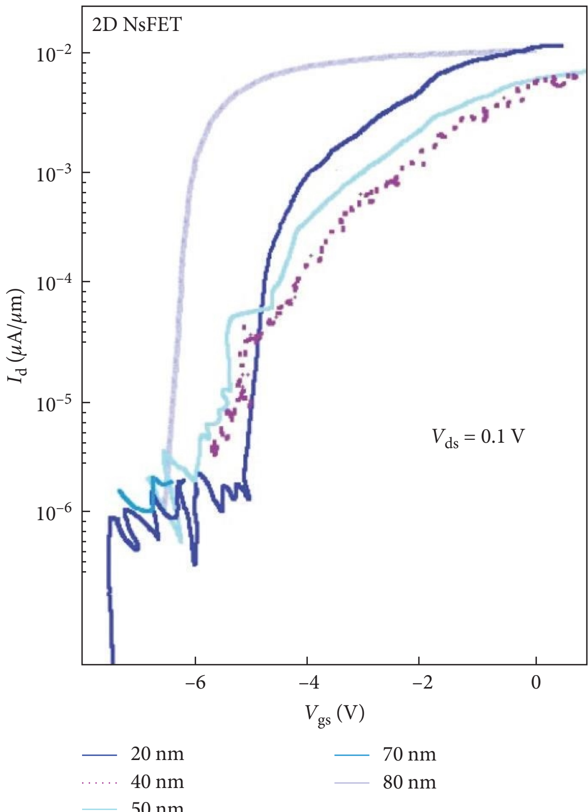

Figure 6: Transfer characteristic of simulated 2D NsFET.

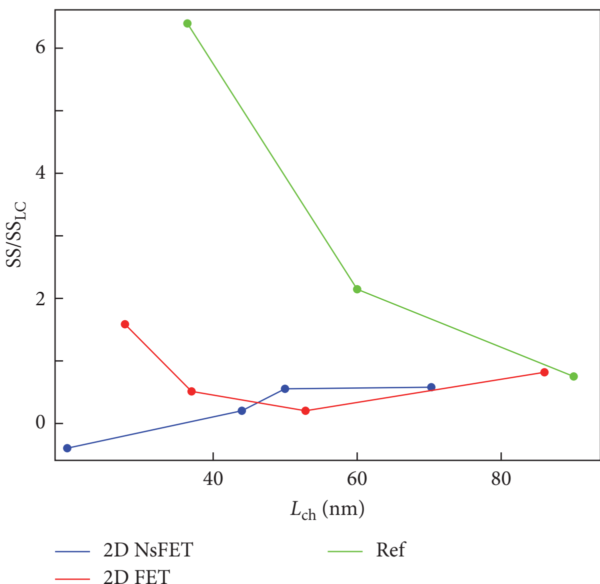

Figure 7: Comparison of subthreshold swing for simulated NsFET with conventional 2D FET.

$$SS\left(\frac{mV}{dec}\right) = \left[\frac{\partial(\log_{10}(I_D))}{\partial V_{GS}}\right]^{-1}. \quad (2)$$

Figure 8 depicts I_{ON}/I_{OFF} comparison plot for conventional 2D FET with proposed NsFET for different channel length. The ratio shows 10^5 range for proposed NsFET with channel length of 20 nm, which shows that proposed device can be used for high-switching applications which even more better for reference [32].

5. Conclusion

Self-heating effects and SCEs are unattractive side effects of multigate devices such as gate-all-around nanowire-FETs and FinFETs, which limit their performance and cause reliability issues. For CMOS technology nodes that are evolving,

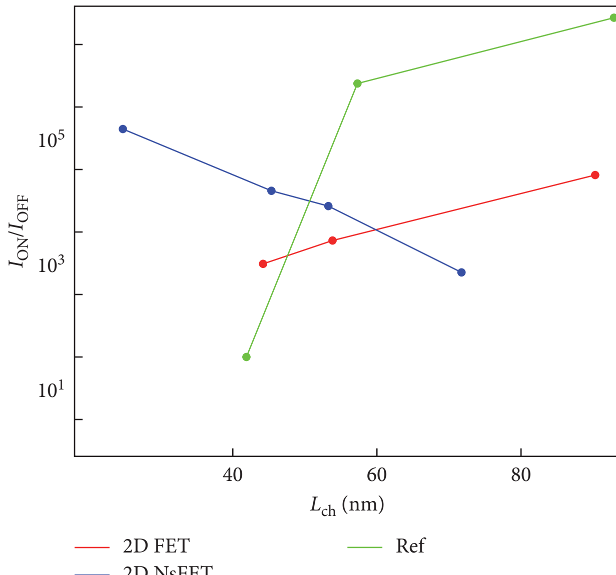

Figure 8: Comparison of I_{ON}/I_{OFF} for simulated NsFET with conventional 2D FET.

this study recommends the adoption of the innovative NsFET. A quick introduction to the roadmap to the sub-nm regime and electronic market is provided alongside design guidelines and basic measurements for the sub nm node. According to the proposed silicon-based NsFET, the device has an I_{ON}/I_{OFF} ratio of more than 10^5. The results were confirmed and obtained successfully for low-power and high-switching applications. The V_{th} tends to fall as NS widths rise, resulting in a reduction of subthreshold efficacy. Furthermore, the performance of the suggested device, such as SS and I_{ON}/I_{OFF}, was investigated using a typical 2D FET. As a result, the NsFET presented here could be a contender for ultra-low power and high-speed switching applications.

Data Availability

The data used to support this study are included within the article.

Ethical Approval

This article does not contain any studies with human or animal subjects.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

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